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Laser Lithography of Monolithically-Integrated Multi-Level Microchannels in Silicon

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The trend toward ever-increased speeds for microelectronics is challenged by the emergence of heat-wall, leading to the faltering of Moore's Law. A potential solution may be integrating microfluidic channels into silicon (Si), to deliver controlled amounts of cooling fluid and regulate hot spots. Such meandering microfluidic channels within other transparent materials already played significant roles, including in biomedical and sensor applications; however, analogous channel architectures do not exist in Si. Here, a novel method is proposed to fabricate buried microchannel arrays monolithically integrated into Si, without altering the wafer surface. A two-step, laser-assisted subtractive removal method is exploited, enabling fully-buried multi-level architectures, with control on the channel port geometry, depth, curvature, and aspect ratio. The selective removal rate is 750 µm per h per channel, and the channel inner-wall roughness is 230 nm. The method preserves top wafer surface roughness of 2 nm, with significant potential for 3D integrated systems.

1. Introduction

Microchannel fabrication methods enable diverse advances in multiple fields.[1–5] These include state-of-the-art biomedical research,[6,7] micro-optical systems,[8] optofluidic sensors,[9–11] lab-chip systems with filters, mixers, sorters,[12,13] and novel microfluidic-integrated platforms.[14,15] Conventional techniques, such as photolithography, reactive ion etching, and electron-beam lithography, have been used to create microchannels positioned over the material surfaces. An emerging paradigm challenging the existing architectures is exploiting 3D microchannel networks to attack the notorious heat wall problem of electronics.[1,16] The success of this paradigm for Si microelectronics would require the creation of microchannels buried inside the bulk (subsurface) of the wafer, to be positioned right below surface hot spots.[17] Unfortunately, conventional methods cannot be used to create channels in Si without altering its top surface. In addition, available techniques require complicated steps, extensive expertise, and expensive infrastructure, precluding wider adoption even for surface fabrication.[1] Achieving high throughput is a further challenge.[18] An alternative direction is afforded by laser-ablation-based lithography.[18–20] However, these methods are also restricted to creating the channels on the surface.

Significant efforts have been directed toward overcoming this architectural challenge to position microchannels directly and inside the bulk of Si with high control.[1,21–24] So far, developed methods may broadly be classified as multi-wafer methods, which rely on bonding two or more chips carrying the surface channels.[1,23,24] Since the microchannel fabrication step is based on conventional methods, these approaches inherit the same challenges. Indeed, the cost and complexity may even be higher due to post-treatment steps, such as alignment and bonding.[23,24] Thus, currently, there is no monolithically-integrated solution for creating microchannel networks inside Si, affording multi-dimensional control.[25]

In contrast, fabrication of buried microchannels has been possible in other materials, such as wide bandgap materials, including sapphire, silicon carbide, and numerous glasses.[26–32] These methods exploit ultrafast-laser-induced subsurface modifications created with 3D control inside the volume. The modifications are usually removed with selective chemical etchants, enabling the fabrication of multi-dimensional arrays with 3D control.[10,33,34] The variations of the various laser processing scenarios include "Femtosecond Laser Irradiation followed by Chemical Etching" (FLICE) and "Water-assisted Femtosecond Laser Drilling" (WAFLD).[35,36] The direct-laser writing nature dispenses with any masks and expensive equipment. Further, fabrication quality and scalability can be improved with emerging optical techniques, including spatial and temporal beam shaping,[36,37] using bursts of laser pulses,[23,38,39] and chemical advances, such as optimized etching protocols.[26,40,41] We posit

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that the translation of this capability to Si is possible. Considering that Si is critical for multiple industries, including microelectronics, Si-photonics, and micro-/nano-electromechanical systems (MEMS/NEMS),[42,43] the 3D fabrication capability holds significant promise toward monolithically-integrated applications through translating biomedical analysis,[13,44] lab-chip systems,[45] and biosensors[15] directly to Si chips. Further, microfluidic networks hold significant potential for the heat management of systems through carrying cooling fluids to hot spots, as illustrated by state-of-the-art heat extraction performance in Gallium Nitride electronics.[1] Motivated by such diverse potential, we aim to establish a versatile multi-level microchannel fabrication method in Si without altering the top/bottom wafer surface.

In laser ablation, the architecture is immediately constrained by the interaction of laser pulses on the wafer surface, leading to shallow trenches or grooves, with 2D-constrained fabrication. During the process, a significant portion of the surface material is removed, wasting valuable chip area. In contrast, here, we exert control directly inside the material, preserving the surface. In order to do so, we exploit infrared laser pulses, where Si is transparent. The nonlinear laser interactions inside the bulk induce localized micro-modifications in Si, affording strong depth control.[2] It has been shown that this mode of laser writing can be used to fabricate thru-Si vias.[2] However, the dimensional barrier is yet to be overcome for creating monolithically-integrated multi-level channel arrays. Here, we establish such a method, with precise control on dimension, position, and geometry within the wafer.

The method involves two steps, 1) 3D laser-writing of a template for the multi-level microchannel array and 2) selective chemical removal of the laser-modified areas. The demonstrated advances include the creation of buried microchannel arrays, concurrent fabrication at multiple depths, nonlinear geometries such as meandering, curved channels, strong control on the channel port geometry, and high-aspect-ratio fabrication capability. During the etching process, subsurface channels are created in parallel, thus the method is strongly scalable. In addition, we preserve the top and bottom surfaces during the entire process (roughness, Ra = 2 nm), implying significant potential for further integration with conventional Complementary-Metal-Oxide (CMOS)-based technologies. This set of advances constitutes a monolithically-integrated, large-volume, and multi-level fabrication paradigm for Si.

2. Results

2.1. Monolithically-Integrated Microchannel Arrays

The multi-level fabrication paradigm is illustrated in **Figure 1**. We exploit a nanosecond-pulsed infrared laser at the wavelength of 1.55 µm, where Si is transparent, thus, the beam propagates without surface effects (Experimental Section). Within the bulk, two-photon absorption and free-carrier absorption processes trigger self-focusing of the pulse, resulting in localized energy delivery at the microscale.[2] This, in turn, leads to localized material modification in Si.[25,46] Through controlling the location of modifications in 3D, one can form the template for an array of microchannels at different depths (Step 1). The laser-lithography is performed with multiple neighboring subsurface micro-planes (Figure 1a, inset). The subsurface modifications may be extended to the surface or, optionally, accessed simply by dicing the sample. In the next step, the modified parts are simultaneously exposed to a selective etchant (Step 2), where these sections and limited amount of crystal in between are removed, boosting the fabrication throughput (Experimental Section). The top and bottom surfaces are protected with photoresist throughout the process. The robust depth control enables multi-level array fabrication, which can laterally extend indefinitely, only to be limited by the range of translational stage or extent of the wafer.

The geometry and coordinate system are defined in Figure 1b. We exploit two modes of laser writing in Step 1. The first is transverse writing modality, where the laser propagates along the z-axis, perpendicular to the sample scanning direction along the y-axis. The second is longitudinal writing modality, where the laser propagates along the y-axis, parallel to the scanning direction. Both approaches are used to exert depth control, simply by changing the location of focus along the z-axis. The scanning electron microscope (SEM) image in Figure 1b-i illustrates three completely open microchannels, created at various depths in Si, using transverse laser writing modality. Here, the channel extent along the z-axis is associated with the Rayleigh length of the laser, and the horizontal extent is controlled by a set of Ω consecutive micro-planar modifications created with a spacing of Λ. In this case, the laser pulse energy (E_p) is 4.3 µJ, the spacing between consecutive modifications is Λ = 11 µm, and the chemical etching time is 2 h. The cross-section geometry of the channels is controlled with laser scanning over the x–z plane. We found that Λ and E_p are essential parameters for avoiding excess stress accumulation within the wafer, as will be detailed later. After the fabrication process, the photoresist is removed. A representative SEM image of the top surface already indicates preserved morphology (Figure 1b-iii). Next, we will analyze quality metrics in more detail.

2.2. The Quality Metrics of Microfabrication

As we explored the fundamentals of lithography, we now focus on the quality metrics, *i.e.*, roughness values for the microchannel inner wall and top wafer surfaces after fabrication, chemical preservation of the wafer surface, and fabrication throughput. These will be followed by demonstrations of architectural control within the bulk. We find that the channel inner wall roughness, as measured in arithmetic average of profile height (Ra), depends on the spatial profile of the laser. While microchannels fabricated with a Gaussian beam profile have wall roughness of Ra = 10 µm, one may exploit spatially-modulated beams for lower roughness values. We demonstrate a proof-of-concept fabrication based on Bessel-beam laser writing,[47] and achieve an inner wall roughness of Ra = 0.23 µm (**Figure 2a**). After the selective removal step, this channel is diced at its center and evaluated with laser scanning microscopy (LSM). The imaged area is highlighted in Figure 2a-i, and the associated LSM data is shown in Figure 2a-ii. The reduced roughness is associated with an improvement in the laser-writing step. The non-diffracting nature of the Bessel beams enables modifications with sub-micron feature sizes (>100 nm) and with ≈200 µm axial length.[47,48] The longitudinal modality enables high-resolution linear laser-written tracks, which results

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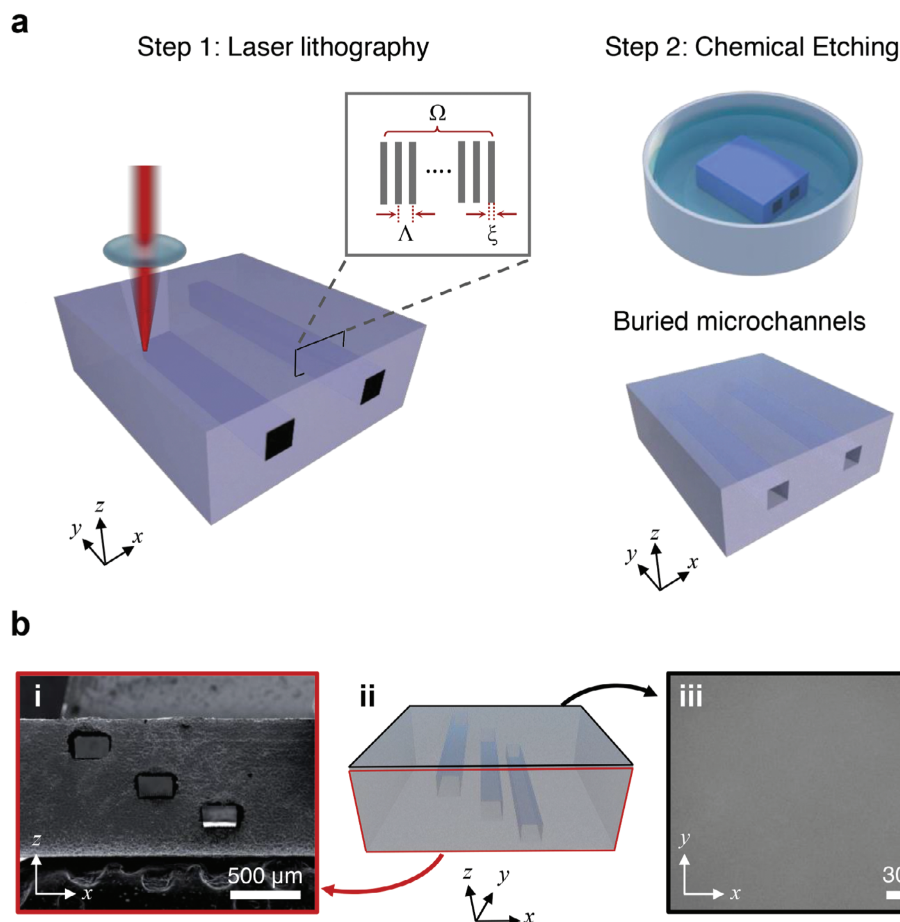

Figure 1. Methodology of fabricating fully-buried microchannels in silicon. a) The schematic represents the concept of monolithically-integrated microchannel fabrication in Si. Step 1: Laser lithography buried inside Si. Subsurface micro-planes of thickness ξ and separation Λ are written in Si as Ω distinct planes. Transverse writing modality is shown in the schematic. Step 2: Selective chemical removal of the laser-written subsurface regions, revealing the microchannel arrays. b) Multi-level array with surface preservation. (i) Scanning electron microscope (SEM) image of the sample cross-section with three open microchannels positioned at 190 µm, 460 µm, and 700 µm below the surface. (ii) Schematic shows a Si sample with buried microchannels and an unaltered surface after Step 2. The red border represents the cross-section on the *x*–*z* plane; the black border represents the sample surface on the *x*–*y* plane. (iii) SEM image shows the preserved Si surface on the *x*–*y* plane, with three microchannels buried underneath.

in linear microchannels with increased aspect ratios and lower Ra values. We will mainly use Gaussian beams for increased architectural control, e.g., curved channel fabrication, and also for higher effective etching rates.

An important consideration for potential surface/subsurface functional integration would be preserving the top wafer surface. This is automatically satisfied in Step 1, as the laser propagates without surface alteration during transverse writing; and does not even interact with this surface in the longitudinal writing modality. In Step 2, the surface is protected with photoresist coating (Experimental Section). We evaluate the roughness after Step 2 using an optical profilometer device (Zygo NewView 7000). We first measure the surface roughness of a wafer carrying a buried and completely opened channel after removing the photoresist (Figure 2b-i), then, compare this with a pristine wafer (Figure 2b-ii). The roughness value for the former is measured as 2.2 nm, whereas the latter is 2.0 nm. The result corroborates the preceding SEM analysis (Figure 1b-iii), showing the surface is preserved. We further evaluate the chemical composition of the samples with energy-dispersive X-ray spectroscopy (Figure S1, Supporting Information). Our measurements do not indicate a discernible difference between the surfaces, indicating strong surface preservation. These results suggest that there is significant potential for integrating surface functionality with subsurface microfluidics.[1]

The fabrication throughput is controlled by the rate of etching. We first evaluate this for the simplest case, *i.e.*, using a single laser scan. We measured the opening rate for a single laser track (ξ = 3 µm) as 189 µm h^{-1} from one side. This may be scaled to uniformly-separated micro-plane tracks, each fabricated with a distance of Λ from its neighbor. The arrangement increases the surface area for the chemical reaction, significantly improving the throughput. For such arrays, the opening rate for the entire channel is taken as the effective rate. We performed systematic experiments to optimize this value, considering the critical parameters of inter-plane separation (Λ), the number of planes (Ω), and the laser pulse energy (E_p). The measured etching rate is given as a function of E_p in **Figure 3a**, for Λ = 11 µm, Ω = 16.

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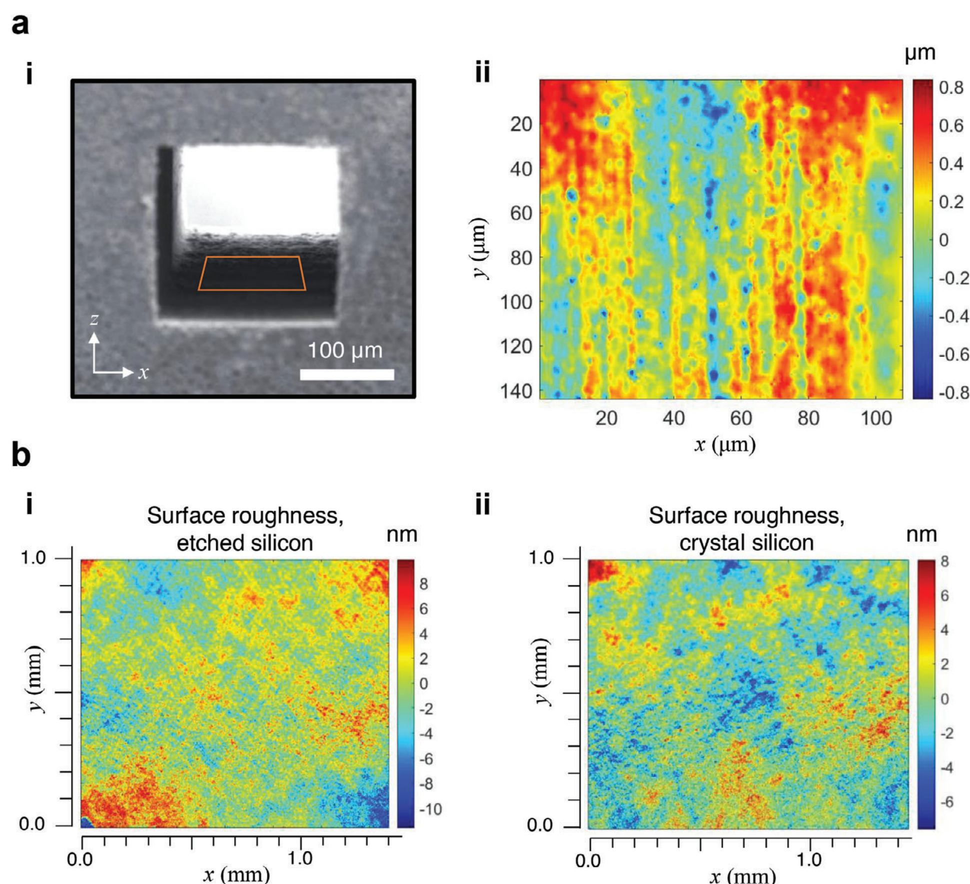

Figure 2. Characterization of the wafer surface and microchannel inner wall. a) Characterization of the channel inner-wall roughness from a high-aspect-ratio, completely opened buried microchannel. (i) SEM image of a microchannel from the *x*–*z* cross-section plane. The orange border represents the analysis area for laser scanning microscope (LSM). (ii) LSM data from the inner wall indicates inner wall roughness of Ra = 0.23 µm. b) Characterization of the top sample surface. (i) The optical profilometer data indicates that the surface has a roughness of 2.2 nm following Step 2. (ii) The optical profilometer data for pristine silicon indicates a roughness of 2.0 nm, comparable to that of (b-i).

The observed monotonically increasing trend may be expected, as higher E_p produces thicker and longer building blocks. We identify three main operation regimes in Figure 3a. For a given Λ, lower E_p values result in higher wall roughness, mainly when ξ is significantly lower than Λ (Regime 1, blue-shaded area). This may be reduced by decreasing Λ, if needed. Conversely, assuming high E_p results in stress accumulation due to wider laser tracks, creating undesired cracks inside Si (Regime 3, pink-shaded area). Thus, intermediate E_p values are identified as ideal for microfabrication (Regime 2, white area). In this regime, we achieved a significant etching rate of 680 µm h^{-1}, measured from a single entry port (E_p = 4.3 µJ). The inter-plane separation Λ is also observed to influence the optimal fabrication regime (Note S2, Supporting Information).

In order to further increase the throughput, we selected E_p = 4.3 µJ, Λ = 11 µm, and optimized the material removal rate for the number of laser-written subsurface planes (Ω). Figure 3b shows the measured etching rate for channels created with Ω, ranging from 4 to 24. Since the total reaction surface area is proportional to Ω, one observes higher rates with increased Ω. This conclusion may also be generalized to channels fabricated with different port geometries. However, increasing Ω beyond a specific value results in stress accumulation within Si, potentially resulting in structural deformation. Thus, remaining within the optimal fabrication regime, Λ = 11 µm, E_p = 4.3 µJ, and Ω = 20, the etching rate is measured as 750 µm h^{-1}. We note that this value is comparable to the highest etching rate recorded for glass, 820 µm h^{-1}.[49] Assuming the preceding lithography parameters, typical microchannels in Si of 250 µm × 200 µm port size, and 1.7-mm length require about 1.2 h to open completely.

2.3. Control on Geometry and Architecture

Next, we showcase subsurface microchannels with robust geometrical control. We begin with high-aspect-ratio open channels of 1-mm length (Figure 3c). While the extent along the *z*-axis is given by the Rayleigh length of the laser, the channel width can be dynamically controlled with the Ω parameter. A representative set of channels are shown for Ω = 20 (Figure 3c-i) and Ω = 10 (Figure 3c-ii), achieving an aspect ratio of 5 and 17, respectively. Similarly, we fabricated channels of 250 × 200 µm^2 cross-section, with up to a length of 5 mm, achieving an aspect ratio of 25. In comparison, to the best of our knowledge, the highest aspect ratio

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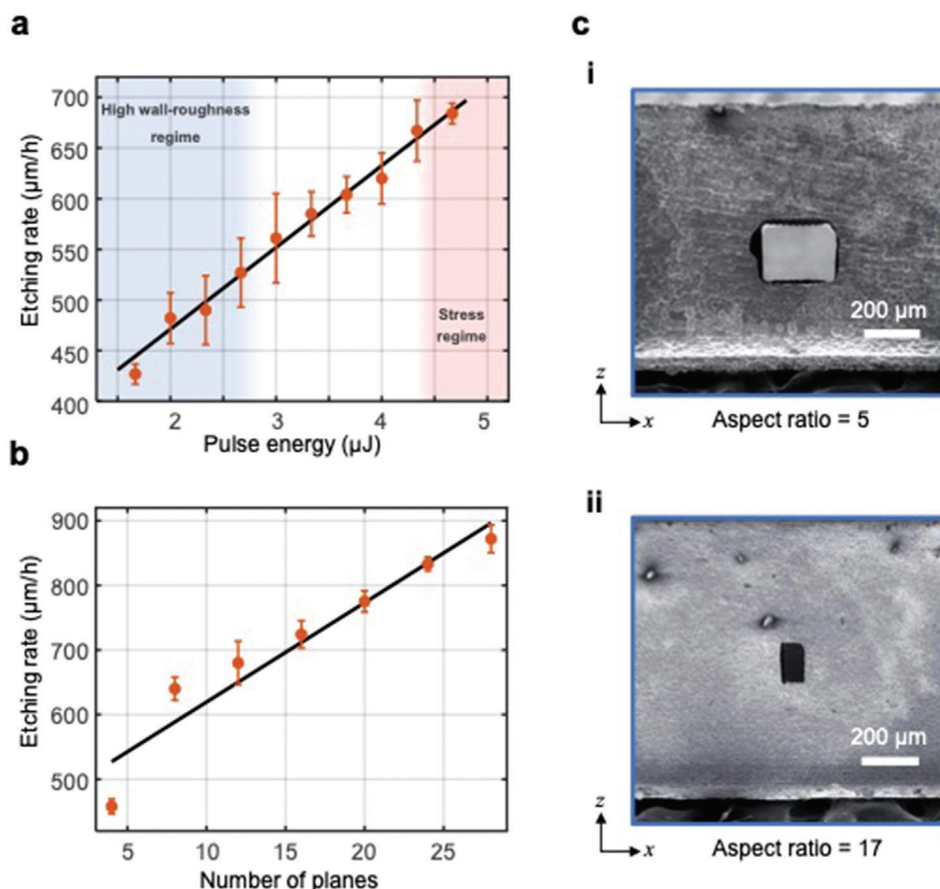

Figure 3. Etching rate analysis and control on channel aspect ratio. a) The effective etching rate is given as a function of pulse energy, E_p, for $\Omega = 16$ micro-planes and plane separation of $\Lambda = 11$ μm. The depth of microchannels is 540 μm, fabricated with 2 h. etching. Three main operation regimes are identified. Regime 1 assumes low E_p, creating relatively high roughness on channel walls. Regime 3 assumes high E_p, resulting in stress accumulation and undesired subsurface cracks. The intermediate E_p values indicated with white color identify the ideal operation regime. b) The etching rate as a function of Ω, for $E_p = 4.3$ μJ. The error bars in (a,b) correspond to standard deviations. c) SEM images from the *x–z* plane, indicating control on the microchannel aspect ratio, created with $\Omega =$ (i) 20 and (ii) 10. All data assumes Gaussian beams and transverse laser writing modality. Scale bar: 200 μm.

achieved via laser ablation on Si is limited to 10, with a channel length of 100 μm.[18] The uniformity of such elongated channels is further discussed in Note S3 (Supporting Information).

While the preceding subsurface microchannels have rectangular ports, one may also fabricate different port geometries. Preserving the aspect ratio of 25, we fabricated microchannels of circular, square, and triangular port shapes (**Figure 4**). These are created by exploiting spatially-modulated laser beams with nondiffracting nature, i.e., Bessel beams,[47,50] for higher resolution. Due to the longitudinal writing modality, the laser can be scanned

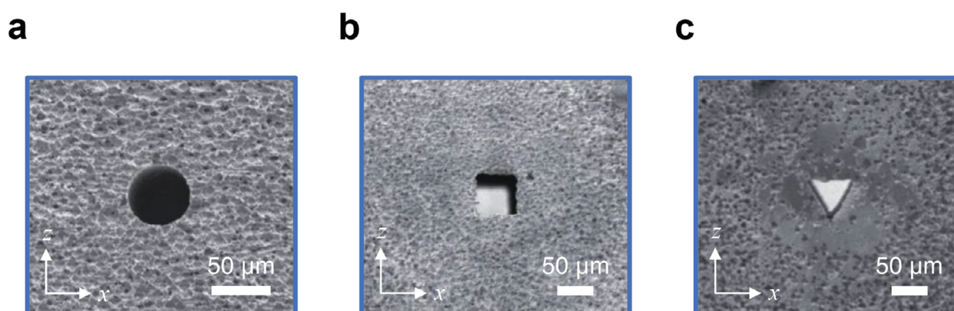

Figure 4. Control on the port geometry of channels. a) Circular, b) square, and c) triangular-shaped microchannel ports. The channels are created by scanning the nondiffracting Bessel beam over the *x–z* plane in longitudinal modality. The SEM images are acquired from the *x–z* plane. Scale bar: 50 μm.

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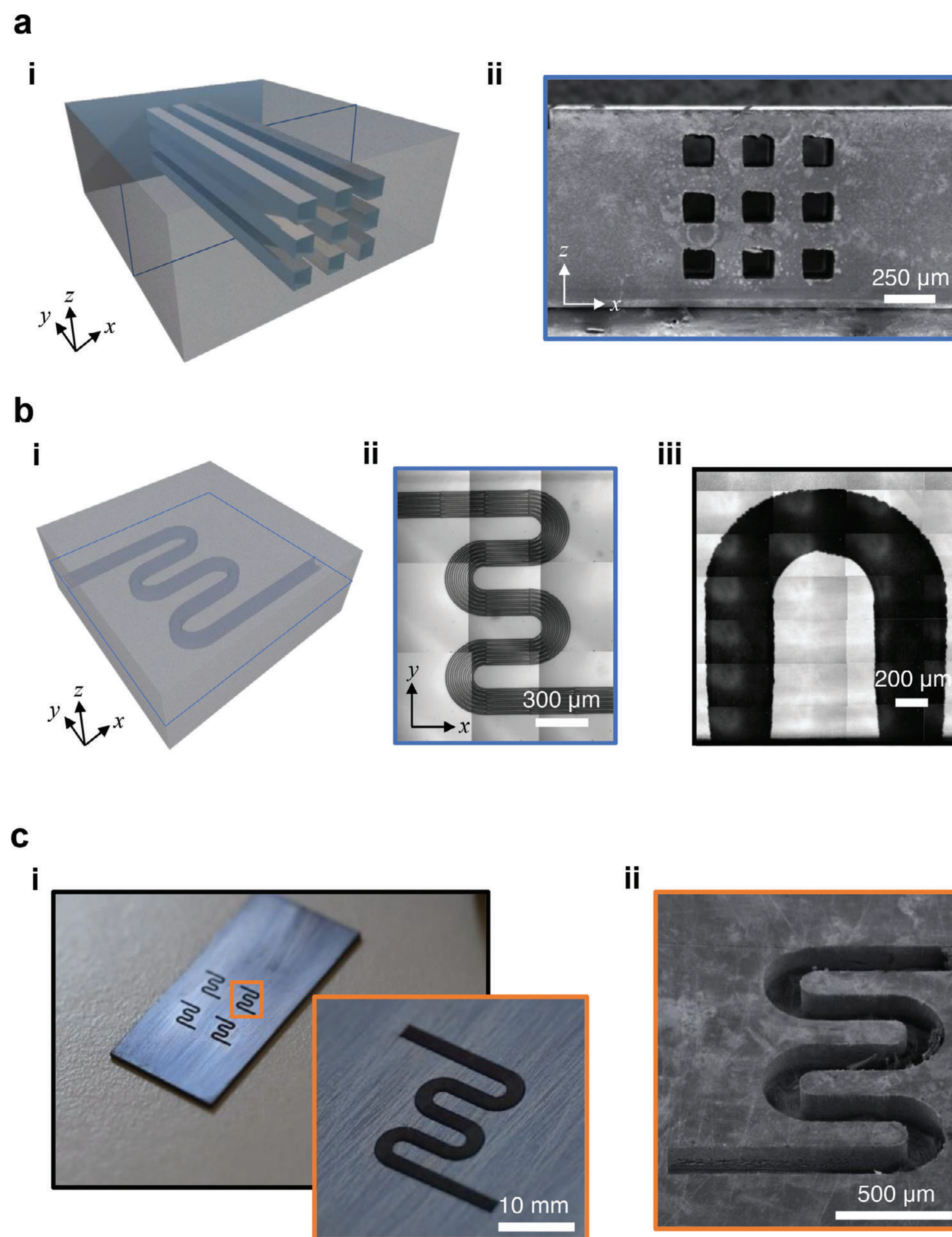

Figure 5. Multi-level and curved architectures. a) Multi-level subsurface array. (i) Color-coded schematic of a 3 × 3 array, indicating cross-section on the *x*–*z* plane. (ii) SEM image from the *x*–*z* cross-section shows a 3 × 3 array in 1-mm-thick Si. Completely opened microchannels extend 1.2-mm along the *y*-axis. b) Curved architectures in Si. (i) Schematic of a curved subsurface pattern. (ii) Infrared microscopy image of laser-written curved pattern with multiple laser tracks (E_p = 3.6 µJ and Λ = 12 µm). (iii) Infrared image of a buried open microchannel after Step 2. c) (i) High-definition camera image of a surface array. Inset: Close-up view of an individual channel. (ii) Representative SEM image of high-aspect-ratio curved channel from the set shown in (c-i). All architectures are created with transverse laser writing modality and Gaussian beams.

over the *x*–*z* plane to create virtually any shape over this plane, preserving the high aspect ratio. The method has the added benefit of significantly reduced cross-sectional area, e.g., 50 × 50 µm^2 for the square-shaped port (Figure 4b).

Further exploitation of the third dimension is possible with architectural control. We envision creating an array of open channels within Si, preserving the top and bottom surfaces (**Figure** 5a-i). This can be achieved by controlling the positions and depths of individual microchannels. We employ one-by-one bottom-to-top writing with transverse laser writing (E_p = 2.9 µJ, Λ = 10 µm, and Ω = 14), in order to create a state-of-the-art 3 × 3 array of channels in 1-mm-thick Si (Figure 5a-ii). This arrangement can easily be generalized to other port shapes and aspect ratios. A precursor to advanced control and heat-exchange capabilities based on arbitrarily shaped channels in Si is creating curved microchannels. Currently, there is no existing technique to create buried, open microchannels with curved architectures. To this end, we exploited our laser-fabrication

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approach and created the first such curved channels in Si (Figure 5b-i). A computer-generated code for stage control is used to scan uniformly-separated and curved laser tracks in volume (Figure 5b-ii). The transverse laser writing modality (E_p = 4.7 μJ, Λ = 10, depth = 490 μm) enables virtually complete freedom on the channel shape over the *x*–*y* plane. After the chemical etching step, the buried curved channels are completely opened (Figure 5b-iii). A simple modification of the method allows one to create surface curved channels or deep trenches. If one polishes down to laser-written areas and then uses the same etching protocol, the entire curved shape or arrays of curved channels can be created on the surface (Figure 5c). Achieving such deep structures over Si would be a challenging endeavor with conventional methods. Thus, we established a comprehensive laser-fabrication approach that achieves a rich set of channel architectures in Si, with virtually any shape on the plane perpendicular to the laser axis (complete 2.5D control).

In summary, we introduced a unique fabrication method for monolithically-integrated multi-level microchannel arrays in Si. These are created in rich geometries and architectures with potential applications from microsystems to electronics. Subsurface microchannels of port sizes down to 50 × 50 μm^2 are fabricated, with a channel inner-wall roughness of down to 230 nm. The channels may also be created with different port shapes, including circular, triangular, or rectangular geometries. Multilevel (3 × 3 array form) and curved fabrication capabilities are established buried inside the wafer, providing significant fabrication flexibility. An etching rate of 750 μm per h per channel is evaluated, enabling a significant channel aspect ratio of 25 for Si. We emphasize that the method preserves the top wafer surface during and after fabrication, which provides a robust fabrication capability for silicon. An elementary cooling demonstration is given in Note S4 (Supporting Information), where passing cooling water through a completely buried channel rapidly reduces the surface temperature. Future scaling of the technique may enable optofluidic and Si-photonics applications, and on-chip/inchip integrated systems. An exciting future direction would be using meandering channels as heat exchangers for multi-level Si-electronics; akin to blood vessels regulating the heat of the human brain, in order to help extend Moore's law by increasing clock rates.

3. Experimental Section

Materials: One millimeter thick p-doped <100> type Si with resistivity of 1–10 Ω.cm and 1-mm-thick p-doped <111> type Si sample with resistivity of 1–10 Ω.cm were purchased from Siegert Wafer, Germany. Copper (II) nitrate trihydrate [$Cu(NO_3)_2$*3(H_2O)], Hydrofluoric Acid [HF, %40], and AZ-5214E photoresist (PR) were purchased from Merck, Germany. Nitric Acid [HNO_3, %65], and Acetic Acid [CH_3COOH, %100] were purchased from Sigma–Aldrich, United States.

Laser Lithography Inside the Wafer: A home-built nanosecond laser setup was used for laser writing. The details of the system are described elsewhere.[2,46] Briefly, the laser had a pulse length of 10 ns, maximum power of 9 W, and 150 kHz repetition rate with a variable rate. The output wavelength λ = 1550 nm was in the transparency window of Si. The laser power was controlled with a quarter-wave plate (QWP) and a half-wave plate (HWP). A polarizing beam splitter (PBS) was used for creating *p*-polarized light. The beam was expanded and collimated using a pair of lenses, L_1 (f_1 = 15 mm) and L_2 (f_2 = 35 mm), which was then projected onto a Spatial Light Modulator (SLM) for experiments with Bessel-type modulation.[47,48] A liquid-crystal-on-silicon (LCOS) SLM with 792 × 600 pixels and 20 μm pixel size (Hamamatsu, LCOS-SLM, X10468-08) was used. The SLM was used as a mirror for Gaussian beam experiments. The reflected beam was demagnified using a 4-*f* system with lenses L_3 (f_3 = 125 mm) and L_4 (f_4 = 100 mm), reducing the beam diameter to the aperture of the final aspheric lens (*f* = 4.5 mm). The laser was focused inside Si and scanned with a speed of 1 mm s^{-1} (Step 1, Figure 1a). The sample was mounted on a nano-positioning stage (Aerotech, ANT130-XY, ANT95-L-Z), enabling high-resolution 3D scanning. The scans were performed with longitudinal or transverse writing modalities. Experiments were performed at room temperature and in an ambient atmosphere. The focused beam induces nonlinear interactions within the bulk,[25] creating localized modifications in Si. These, in turn, form the 3D templates of channel arrays to be revealed in Step 2.

Selective Chemical Removal and Microchannel Fabrication: The laser-modified regions buried inside the sample were selectively removed with an HF-based solution, to reveal the buried microchannels. This protocol was shown to be effective for the fabrication of surface micro-pillar arrays upon laser irradiation.[2] The etchant consisted of several chemicals with the following composition: H_2O (15 mL), $Cu(NO_3)_2$*3(H_2O) (3 gr), HF (36 mL), HNO_3 (25 mL), and CH_3COOH (24 mL). A surface passivation step before the etching process was employed, such that the surface of the wafer remains unaltered during material removal. For this purpose, the sample was first drop-casted with AZ-5214E photoresist (PR), and hard-baked at 120 °C for 5 min. After 2 h, the selective etching protocol was applied. The resist was found to be effective for 75 min during the process. For experiments requiring longer periods[51] and the creation of high-aspect-ratio channels, a time-multiplexed etching process was employed, with alternating passivation and chemical etching steps (70 min). The selectivity of the etchant is evaluated in Note S5 (Supporting Information).

Surface and Inner Wall Characterization: To characterize the physical and chemical morphology of the top surface of the sample, an optical profilometer device (OPD, Zygo NewView 7000) with an axial resolution of < 1 nm; and an energy dispersive X-ray spectroscopy (EDAX) were used. A laser scanning microscope (LSM, VKX 100) with an axial resolution of 5 nm was used to evaluate the inner wall roughness of channels.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors are inventors on a patent application (TR/2023/003165) by Bilkent University based on the work here.

Author Contributions

M.A.T. and R.A.S. contributed equally to this work. O.T. designed the research. Experiments were performed by M.A.T. and R.A.S. R.A.S., M.A.T., and O.T. interpreted the results. All authors contributed to the writing of the manuscript.

Data Availability Statement

The data that support the results of this paper are available within the manuscript or supplementary information.

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3D microfabrication, laser lithography, microchannels, nonlinear laser interactions, silicon

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